Strained Si NMOSFETs for High Performance CMOS Technology

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Abstract

Performance enhancements in strained Si NMOSFETs were demonstrated at L_{eff} <70 nm. A 70% increase in electron mobility was observed at vertical fields as high as 1.5 MV/cm for the first time, suggesting a new mobility enhancement mechanism in addition to reduced phonon scattering. Current drive increase by ≥35% was observed at L_{eff} <70 nm. These results indicate that strain can be used to improve CMOS device performance at sub-100 nm technology nodes.

Introduction

Due to the lattice mismatch, a pseudomorphic layer of Si on relaxed SiGe is under biaxial tensile strain, (Fig. 1) which modifies the band structure and enhances carrier transport [1]. In an electron inversion layer, the subband splitting is larger in strained Si because of the strain-induced band splitting in addition to that provided by quantum confinement (Fig. 2). The ground level splitting ($E_0(\Delta_4) - E_0(\Delta_2)$) in a MOS inversion layer at 1 MV/cm transverse field is ~120 and ~250 meV for unstrained and strained Si, respectively. The increase in energy splitting reduces intervalley scattering and enhances NMOSFET mobility, as demonstrated at low (<0.6 MV/cm) [2, 3] and higher (~1 MV/cm) vertical fields [4]. The scaled device g_m is also improved due to the reduced density of states and enhanced non-equilibrium transport [5].

In this work, we fabricated strained Si NMOSFETs with sub-70 nm L_{eff}. These devices exhibited enhanced mobility at vertical fields as high as ~1.5 MV/cm and increased current drive, indicating promise for the 70 nm technology node.

Device Fabrication

Strained Si and relaxed SiGe layers were grown epitaxially by UHVCVD. The Ge content was graded in steps to form a fully relaxed SiGe buffer layer before a thin (~20nm) strained Si channel layer was grown. XRD analysis was used to quantify the Ge content (15, 20%) and strain relaxation in the SiGe layer. (Fig. 3 shows an example with 13% Ge content.) The strain state of the Si channel layer was confirmed by Raman spectroscopy. Fig. 4 shows a Raman spectrum of a strained Si layer on $Si_{0.8}Ge_{0.2}$, as grown and after 5 min. RTA at 1000°C. The strained Si peak position did not move after RTA, showing compatibility with the critical thermal cycles in a typical CMOS processes.

A standard CMOS process with STI isolation was used to fabricate the devices. Strained Si (SS) and unstrained Si control wafers were processed simultaneously using the same process condition. Fig. 5 shows the XTEM of a fabricated SS NMOSFET with L_{poly} = 110 nm. A 2.2 nm gate oxide grown on strained Si had a uniform thickness and a smooth interface. Identical T_{ox} in the SS and control devices was confirmed by T_{inv} measurements, and resulted in comparable gate leakage characteristics. (Fig. 7.) Arsenic and phosphorus diffusion is enhanced in SiGe while boron diffusion is suppressed. This resulted in a larger gate overlap capacitance (Fig. 6) and a smaller L_{eff} for a given L_{poly} in the SS devices.

Electrical Characterization

The effective mobility μ_{eff} is plotted as a function of vertical effective field E_{eff} in Fig. 8. Split *C-V* measurements were used to determine the inversion carrier concentration for the μ_{eff} and E_{eff} calculations. The E_{eff} range is slightly higher for the SS devices due to suppressed boron diffusion in SiGe leading to higher channel doping. The μ_{eff} of the SS device is well above the universal μ_{eff}, and at least 70% higher than that of the control even at E_{eff}>1 MV/cm. In a technology employing T_{inv} ~1.5 nm and V_{DD} ~1 V, the maximum E_{eff} is not expected to exceed 1.5 MV/cm. The strain-induced μ_{eff} enhancement in Fig. 8 persists for E_{eff} of up to and possibly beyond 1.5 MV/cm, demonstrating its relevance in the sub-70 nm technology nodes. The μ_{eff} enhancement at such high E_{eff} cannot be explained by the improvement of phonon-limited mobility μ_{ph} [6] alone, and indicates that tensile strain may also improve the so-called surface roughness scattering-limited mobility μ_{SR} in NMOSFETs.

Figs. 9 and 10 compare SS and control devices with L_{eff} = 67 nm as determined by a capacitance measurement technique. (A SS device with L_{poly} = 110 nm was compared to a control device with L_{poly} = 80 nm to account for the difference in gate overlap and match L_{eff}.) Narrow devices (W=0.28 μm) were compared to minimize the impact of self-heating [2, 4]. Excellent turn-off characteristics are observed with comparable subthreshold slopes (82 and 85 mV/dec) and DIBL (70 and 80 mV). The V_T of the SS device is lower (~200 mV) in part due to the smaller bandgap and lower conduction band in strained Si. No attempt was made to adjust or match the V_T of the SS and control devices. The smaller bandgap in SiGe and a finite density of epi dislocations lead to larger junction leakage in the SS devices, but not large enough to affect I_{off} for a typical choice of V_T. Fig. 10 shows the output current of the same devices shown in Fig. 9. For a gate over-drive V_{GT} = 0.8 V, the current drive of the SS device is ~35% higher. At a lower V_{GT}, the enhancement is as large as 50%. The smaller output conductance in the SS device indicates a residual heating effect. When self-heating is completely suppressed, the current drive increase may be even larger.

$G_{m,sat}$ vs. DIBL characteristics in Fig. 11 show that the performance enhancement in the SS devices persists for the devices with DIBL >80 mV and L_{eff} < 67 nm. The shortest L_{eff} plotted in Fig. 11 is 45 nm. These results indicate that the strained Si MOSFET is a promising device structure for high performance deep sub-100 nm CMOS technology.

References

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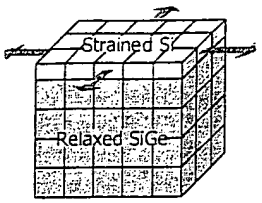

Tensile-Strained Si on SiGe

Fig. 1. Pseudomorphic, strained Si on relaxed SiGe.

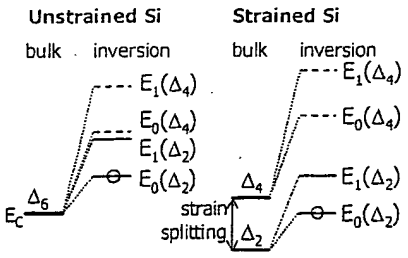

Fig. 2. Splitting of 6-fold degenerate Δ-valleys of conduction band in unstrained and tensile-strained Si inversion layer.

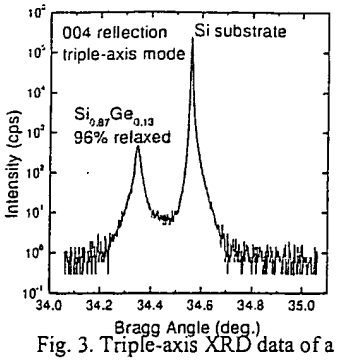

Fig. 3. Triple-axis XRD data of a typical strained Si/SiGe wafer.

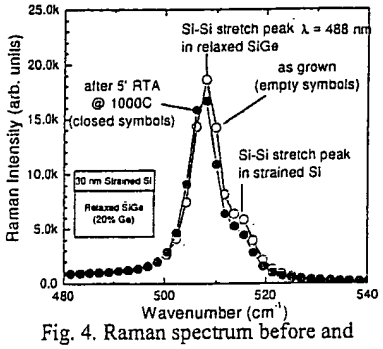

Fig. 4. Raman spectrum before and after RTA at 1000°C. No strain relaxation is observed.

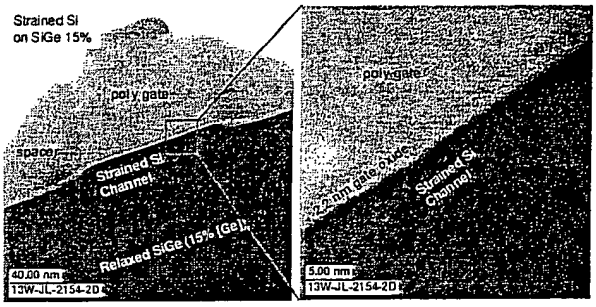

Fig. 5. XTEM of a completed strained-Si NMOSFET. Device region is free of dislocations. Good gate oxide quality with smooth interface is observed.

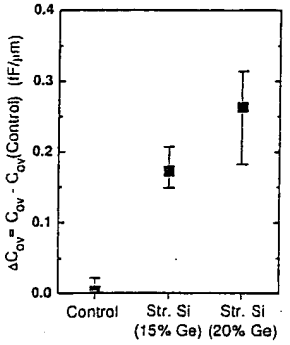

Fig. 6. Gate overlap is larger in SS devices due to enhanced As and P diffusion.

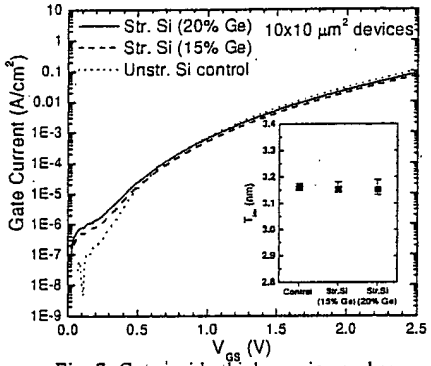

Fig. 7. Gate oxide thickness is nearly identical to control, resulting in comparable gate leakage.

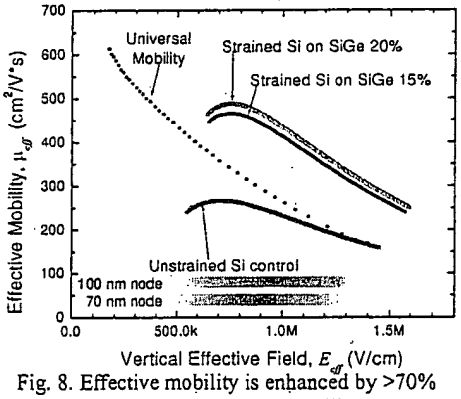

Fig. 8. Effective mobility is enhanced by >70% over the control and universal mobility even at a very high vertical field of >1.0 MV/cm.

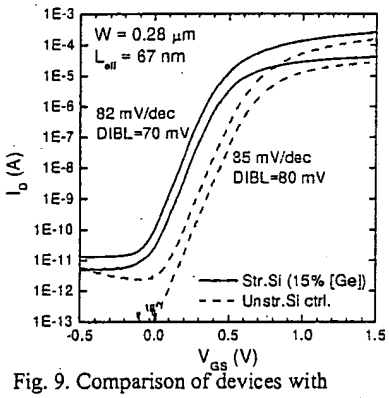

Fig. 9. Comparison of devices with L_{eff} = 67 nm. Sub-threshold slopes and DIBL are comparable for SS and control.

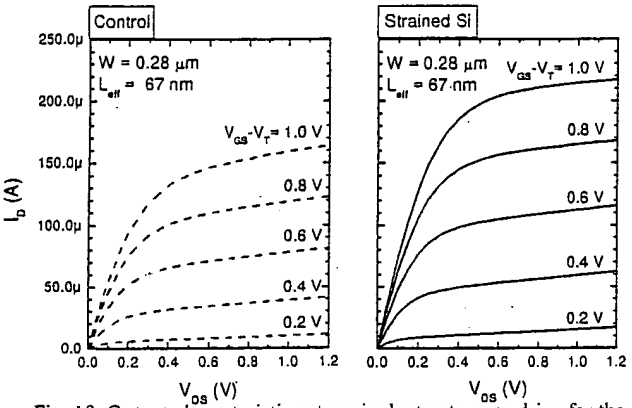

Fig. 10. Output characteristics at equivalent gate over-drive for the devices shown in Fig. 9. Current drive enhancement is observed despite evidence of self-heating in the SS device.

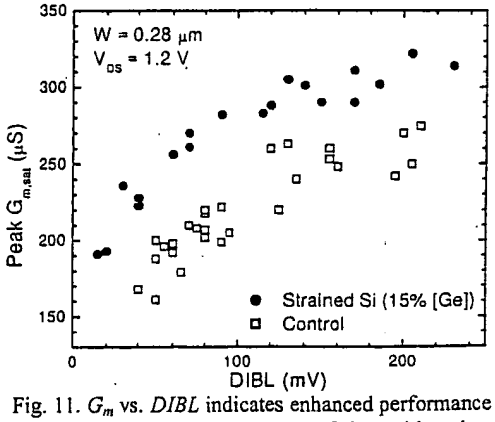

Fig. 11. G_m vs. *DIBL* indicates enhanced performance of strained Si devices across a range of channel lengths.